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U.S. PATENT APPLICATION

Title: **METHOD AND CIRCUIT ARRANGEMENT FOR PICTURE-IN-PICTURE INSERTION**

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Description

Method and circuit arrangement for picture-in-picture insertion

The invention relates to a method for picture-in-picture insertion in accordance with the preamble of claim 1, and to a circuit arrangement for picture-in-picture insertion in accordance with the preamble of claim 9.

In the case of such picture-in-picture insertion (PIP), a smaller insertion picture (small picture) is inserted into a larger main picture. The insertion picture is decimated in accordance with the size reduction and is continuously read into a memory device, older stored pictures being overwritten, and then the insertion pictures are read out in a manner employing synchronization with the main pictures. Accordingly, the read-out speed of the insertion pictures is generally higher than the writing speed. In this case, the main picture and the insertion picture may, in a known manner, be fields which are used for displaying a monitor picture.

At specific phase angles of the rasters of the main picture and of the small picture, the higher read-out speed can lead, inter alia, to the read-out pointer overtaking the write pointer and reading out a previous picture stored in the memory device, with the result that a seam occurs in the middle of a displayed small picture and in part the preceding insertion picture is read out. If both insertion pictures originate from different motion phases, a disturbing effect results since moving objects through which the seam runs are displayed with distortion. If the frequencies of the pictures of the insertion channel and main channel correspond only approximately, the result is slow drifting of the disturbance location, which is found to be particularly unpleasant.

EP 0 739 130 A2 describes a method for eliminating this seam by storing two fields of a small picture, with the result that the field that can be read is always exactly the one which is currently not being written, and, consequently, the read pointer cannot overtake the write pointer. A first and a second memory, which each store a field, are provided for this purpose. This method has the disadvantage, however, that a storage capacity of two insertion pictures or fields is necessary, which entails corresponding costs.

Accordingly, the invention is based on the object of providing a method and a circuit arrangement for picture-in-picture insertion with which the occurrence of a seam in the insertion picture can be prevented in a cost-effective manner and with a relatively low outlay on apparatus.

This object is achieved by means of a method according to claim 1 and a circuit arrangement according to claim 9. The sub-claims describe preferred developments of the method according to the invention and of the circuit arrangement according to the invention.

The invention is based on the concept that it is not necessary, in principle, to store two whole insertion pictures in order to prevent the write pointer from being overtaken by the read pointer. Instead of using a storage capacity of two insertion pictures, a smaller memory device is subdivided into a suitable number of segments, and suitable decision-making is effected to stipulate whether the currently written or the preceding insertion picture is read out.

Consequently, according to the invention - in contrast to the use of two separate memory segments for the currently written and the preceding insertion picture - if appropriate even the currently written insertion picture is read out if it is ensured that the read pointer does not overtake the write pointer.

For this purpose, memory segments which, in particular, are the same size can be cyclically overwritten in a predetermined order since, in particular, good periodicity of the operation can also be ensured by this means. The method according to the invention can be achieved in an advantageous manner by means of the dimensionings according to claims 3 to 6, in which case, in particular, the decision criterion may be chosen according to claim 6.

The invention is explained in more detail below using a number of embodiments with reference to the accompanying drawings in which:

Figure 1 shows a block diagram of a circuit arrangement according to the invention,

Figure 2 shows an illustration of a memory device according to a first embodiment of the invention;

Figure 3 shows an illustration of a memory device according to a second embodiment of the invention.

In accordance with Figure 1, a sequence of main pictures Hi= H1, H2, H3,... are output from a main picture source 1 via a main picture channel 7 to a control device 3. Correspondingly, from an insertion picture source 2, a sequence of insertion pictures Kj = K1, K2, K3,... decimated by a decimation device 12, i.e. reduced in size relative to the main pictures, are output to a memory device S and buffer-stored. In this case, both the main pictures Hi and the insertion pictures Kj are fields which are combined e.g. in a line-offset manner to form the overall monitor picture. Afterward, the sequence of small pictures is read out and forwarded to the control device 3 via an insertion picture channel 8. If an asynchronous main picture source 1 and insertion

picture source 2 are used, the read-out operation of the memory device S is effected in a manner exhibiting synchronization with the main pictures Hi. On account of the decimation, in particular the vertical decimation, the read-out of the insertion pictures Kj from the memory device by the control device 3 takes place more rapidly than the operation of writing to the memory device. The control device 3 combines the main pictures Hi and insertion pictures Kj to form an overall picture which is reproduced on a monitor 6.

1/4 picture-in-picture insertion is assumed below, where the small picture is correspondingly decimated in each case by the factor 2 in the horizontal and vertical. According to the invention, it is provided for this purpose that the memory device has a storage capacity of 1.5 fields (decimated relative to the main pictures) and, in accordance with Figure 2, is subdivided into three memory segments X, Y and Z, all three segments being the same size, i.e. each having a storage capacity of 0.5 field (decimated relative to the main pictures) and being continuously overwritten in this cyclic order. Consequently, a writing start segment I and a second writing segment II are in each case required for a field.

Accordingly, in a first storage operation in accordance with Figure 2 a, a memory area formed from the start writing segment X and the second writing segment Y is written to for the first field K1. The second field K2 is correspondingly written to the start writing segment Z and the second writing segment X in the subsequent storage operation in accordance with Figure 2 b, the start segment of the first field K1 already being overwritten in the process of writing to the second writing segment X. During the third storage operation, the field K3 is correspondingly written to the start writing segment Y and the second writing segment Z in accordance with Figure 2 c. Consequently, at the instant when, in Figure 2 c, the write pointer

is located in the start segment Y, in the location designated by SZ1, the second half of the first field K1 is overwritten, i.e., at this instant, K1 is still partly present, K2 is completely present and K3 is currently being written to the segment Y.

For the read-out operation it must be ensured that, on the one hand, a whole field is read out and, on the other hand, the read pointer does not overtake the write pointer. For this purpose, a decision must be made as to whether the currently written field Kj or the immediately preceding field Kj-1 is read out. Since the difference in the writing and read-out speed is essentially determined by the vertical decimation VD, where VD is a natural number, the decision as to which field is to be read out can be made dependent in each case on VD and on the position of the write pointer in the currently written field. This position of the write pointer generally depends on the position of the small picture in the main picture and hence primarily on the phase angle of the small picture and main picture, the read pointer generally being fixedly coupled to the main picture via the insertion position.

In the case of a vertical decimation of VD=2, the read-out speed is about twice as high as the writing speed, with the result that the read pointer would overtake the write pointer in the currently written field if the write pointer has only written less than half of the field, i.e. is still located in the start segment, as is the case in the position SZ1 in Figure 2 c during the writing of the field K3. Consequently, the preceding field K2 must be read out in this case, i.e. the reading start segment is the writing start segment I of the previous field, i.e. the segment Z according to Figure 2 b. By contrast, at the position SZ2 in Figure 2 c, at which the write pointer is already located in the second writing segment Z, the writing start segment Y can be taken as the reading start segment.

Generally, it can be derived from these considerations that 2*VD-1 segments, each having a storage capacity which corresponds to the quotient of the storage capacity required for an insertion picture and VD, are necessary in order to ensure in each case that either the currently written or the immediately preceding insertion picture can be read out. The total memory space required is thus (2-1/VD) times the storage capacity required for an insertion picture. The saving in comparison with the use of two memory areas for a respective insertion picture thus falls with increasing vertical decimation VD. Since the quotient of reading speed and writing speed can, to a good approximation, be applied as VD, the decisive criterion for the selection of the reading start segment is whether the last segment required for writing the current insertion picture is already being written to.

In the case of 1/9 picture-in-picture insertion, VD=3 and, in accordance with Figure 3, it is necessary correspondingly to choose 2*VD-1=5 segments A,B,C,D and E each having a storage capacity of 1/3 field, with the result that a total storage capacity of 5/3 fields is required. In this case, too, memory segments I, II, III are cyclically overwritten, with the result that the first field is written to the segments A, B and C, the second field to the segments D, E and A, etc. Since the reading speed is about three times higher than the writing speed, the decision criterion to be applied here is whether more than 1/VD = 1/3 of the memory space required for a field remains to be written to. Consequently, in this case, too, the resulting decision criterion is whether the last segment - in this case the third segment III - required for the current field is already being written to.

In addition to the elimination of the seam, it is furthermore possible to eliminate disturbances that may arise as a result of different field positions in

the insertion channel 8 and main channel 7, e.g., in the case of a picture composed of line-offset fields, disturbances between the upper field in the main channel 7 and the lower field in the insertion channel 8. This can be ensured e.g. by storing an additional line, with the result that the lines of the upper field of the insertion channel, despite the dependence on the raster position of the field of the main channel, are always displayed relatively above the lines of the lower field of the insertion channel.